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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,996	06/11/2004	Seetharaman JANAKIRAMAN	TI-36521	3995

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EXAMINER	
YOUNG, BRIAN K	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,996	JANAKIRAMAN ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-46* is/are allowed.

6)☒ Claim(s) *1,2,10,47,48,55 and 56* is/are rejected.

7)☒ Claim(s) *3-9,11-15,49-54 and 57-59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Conclusion

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,10,47,48,55, and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al.

Ono et al disclose (fig.1) a method of converting a sample of an analog signal 10 to a N-bit digital code 75, said method being performed in an analog to digital converter (ADC fig.1 including resolving bits N1 of said N-bit digital code from said sample using one of a first reference voltage 31-1 and is less than N; and resolving bits N2 of an N-bit digital code 75 with a second reference voltage 30-2, and, generating voltages 65 and 66 equivalent to the corresponding N1 and N2 bits. The A/D converter shown in FIG. 1 has several converting stages 60-1, 60-2, . . . , and 61. Analog input 10 to be converted is applied to the first converting stage 60-1 which determines output data 12 of N1 bits. Output data 12 of N1 bits are the most significant bits of a final digital output 75. The first converting stage 60-1 also derives an amplified conversion residue 65 representing a quantization resulting from the conversion performed by the first converting stage 60-1. The amplified conversion residue 65 is derived based on the output data 12 and the analog input 10. The amplified conversion residue 65 is supplied to the second converting stage 60-2 as an analog input.

The second converting stage 60-2 determines output data 13 of N2 bits from the amplified conversion residue 65. The output data 13 of N2 bits is the next significant bits of the digital output 75. The second converting stage 60-2 also derives an amplified conversion residue 66 representing a quantization resulting from the conversion performed by the second converting stage 60-2 same as the first converting stage 60-1. The conversion residue 66 is supplied to the succeeding converting stage.

Thus, each converting stage determines a portion of the bits of the digital output 75 based on a conversion input, and derives an amplified conversion residue representing a quantization conversion residue to a succeeding converting stage as an analog input. The last converting stage 61 determines output data 15 of Nn bits indicating the least significant bits of the digital output 75 from an amplified conversion residue 68 supplied from a preceding converting stage.

3. Claims 3-9,11-15,49-54 and 57-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 16-25 and 26-46 are allowed.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Moreland discloses a pipelined analog-to-digital converter system that converts an analog input signal to a corresponding digital output signal, the successive converter stages that each provides respective bits of said digital output signal and provides a respective residue signal to a succeeding converter stage with the

aid of a respective digital-to-analog converter (DAC) that converts said respective bits with a respective conversion gain that varies in accordance with a respective reference signal wherein at least one of said converter stages includes a main pipeline of main signal-conditioning elements that interact with a respective DAC to process a preceding residue signal into a succeeding residue signal; and

a reference pipeline of reference signal-conditioning elements that mimic at least one of said main signal-conditioning elements wherein said reference pipeline processes a preceding reference signal into a succeeding reference signal.

Tesch discloses an analog-to-digital converter including

input means for receiving analog input signals;

analog-to-digital flash converter means including a resistor array for providing digital signals approximating an input analog signal;

reference means for generating from said approximating digital signals a pair of reference analog signals;

even flash converter means including a capacitor arrays for converting said analog input signals to even digital signals using said pair of reference analog signals;

odd flash converter means including a capacitor arrays for converting said analog input signals to odd digital signals using said pair of reference analog signals;

output means for providing a digital output signal as a combination of said approximating digital signals and either said even or odd digital signals; and

control means for controlling said analog-to-digital flash converter means, said reference means and said even and odd flash converter means to alternate conversion by said even and odd flash converter means.

Lee discloses an audio processing device using multiple DAC's for ADC conversion.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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